DETAILED ACTION

Response to Amendment

The Examiner acknowledges the amendment to claims 1, 7, 8 and 12; the addition of claim 13 and 14; and the cancellation of claim 5 and 6.

Response to Arguments

Applicant's arguments filed 4/28/2008 have been fully considered but they are not persuasive.

In response to Applicants against the reference of Schultz, the Applicant argues that the reference does not disclose “disabling a buffer of a configurable circuit". The Examiner respectfully disagrees with this for the following reasons. While the reference of Schultz discloses P and N transistors to control the impedance of the output signal, the transistors are in pairs (P1 & N1… Pi & N1) therefore, in turning off two transistors (e.g. P4 & N4) the buffer circuits (comprising P4 & N4 transistors in series) is shut off.

Additionally the Applicant argues that " disabling a transistor is different from switching off a buffer... and a transistors is not a buffer, so simply describing how to disable a transistors is insufficient to disclose how the disable the buffer". Again the Examiner respectfully disagrees based on Fig. 2 of the Schultz reference. The Examiner agrees that a single transistor does not comprise a buffer, however the P and N transistor pairs in series are buffers (P1 & N1) and the same transistors pairs can be turned off (independent control of both P and N transistors allows both transistors to be

turned off at the same time), therefore, Schults does disclose how to turn off a buffer circuit as disclosed by claim 1 and the previous rejection of claims 1 and 12 still stand.

Regarding Applicants arguments of claims 7 and 13, “generating at least one control signal for simultaneously switching off a second of buffers”. Schultz discloses a control signal update that is capable of simultaneously switching off a second of buffers (P or N) at the same time by controlling when the updating of the P and N transistors occurs.

Related to claims 7 and 13, the Applicants arguments towards claims 8 and 14 are also not persuasive. The Applicant argues “deriving the control signal from a most significant bit signal", the control signal update is supplied from the Bank DCI 960 which is derived from a most significant bit of comparator 921.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 11 and 12-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Schultz et al. (U.S. Pat. 6,445,245).

Regarding claim 1, Schultz discloses at least one circuit component (903) at which a load is applied (@ pad 943) that can vary during operation (col. 2, lines 37-40)

where the configurable arrangement comprises: load determination means (923 & 960) for determining a load (connected to PAD 943) applied to the at least one configurable circuit component (903) having different fan-in or fan-out (load termination or drive strength) depending on a configuration (impedance matching circuit @ Fig. 11; local DCI 963) of the circuit arrangement (impedance array 211 & 212); adjusting means (963 @ Fig. 9) for switching off a buffer (P & N transistor pairs) connected to the configurable circuit (903) according to the determination of the applied load (@ pad 943) wherein switching off the buffer adjusts a drive capacity (in drive transistors arrays 211 & 212) of the at least one circuit component (buffer 903) to a value less than a maximum drive value (any value where not all transistors of the drive array P1-P15 or N1-N15 are turned on) meeting a delay specification (propagation delay of the signal between integrated circuit elements).

Regarding claim 2, Schultz discloses the determinations means (923 & 960 @ Fig. 9) is configured to determine the load based on configuration information (within configuration memory 1110, Fig 11; detailed drawing of DCI 963) to the circuit arrangement (Fig. 9).

Regarding claim 3, Schultz discloses where the configuration information is stored in a configuration memory (1110 @ Fig. 11).

Regarding claim 4, Schultz discloses where the configuration information comprises a configuration bit stream (col. 15, lines 29-30) defining at least one of an input load and output load (connected to PAD 903) of the at least one component (903).

Regarding claim 7, Schultz discloses where the adjusting means (963 @ Fig. 9) is adapted to generate at least one control signal (update_P / update_N @ Fig. 11; details of 963) for simultaneously switching off a section of buffers (signal controls when P & N transistors get turned on or off).

Regarding claim 8, Schultz discloses where the adjusting means (963 @ Fig. 9) is adapted to derive the control signal (update N/P) from a most significant bit (MSB of update signal) of a selection signal obtained from the determination means (923 &960).

Regarding claim 11, Schultz discloses where the circuit arrangement is a FPGA (col. 1, lines 13-16).

Regarding claim 12, Schultz discloses determining a load (connected to pad 943 @ Fig. 9) applied to at least one circuit component (903) having different fan-in or fan-out (load termination or drive strength) depending on a configuration (impedance matching circuit @ Fig. 11; local DCI 963) of the configurable circuit arrangement; and switching off a buffer (P and N transistors pairs in series) connected to the configurable circuit (903) according to the determination of the applied load (at pad 943), wherein

switching off the buffer (transistor pairs) adjusts a drive capacity (in drive transistors arrays 211 & 212) of the at least one circuit component (903) responsive to the determination step (923 & 960) to a value less than a maximum drive capacity (any value where not all transistors of the drive array P1-P15 or N1-N15 are turned on) while still meeting a delay requirement (propagation delay of the signal between integrated circuit elements).

Regarding claim 13, Schultz discloses further comprising simultaneously switching off a section of buffers (can simultaneously turn off multiple P or N transistors at the same time).

Regarding claim 14, Schultz disclose deriving the control signal (updateP/N) from a most significant bit of a selection signal (MSB of update signal).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schultz et al. (U.S. Pat. 6,445,245) in view of Ajit (U.S. Pub. 2002/0113628).

Regarding claim 9, Schultz discloses that of claim 1 but fails to teach where the adjusting means is configured to vary the threshold voltage of a circuit elements in the arrangement.

Ajit teaches (Fig. 6) changing the transistor threshold voltage by biasing the transistor wells with biasing circuit (401), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the output buffer disclosed by Schultz with the transistor biasing as taught by Ajit for varying the on/off voltage thresholds of the drive transistors.

Regarding claim 10, the combination discloses where the adjusting means (Ajit; 401 @ Fig. 10) is adapted to change at least one bias voltage (PMOS transistors) in response to the determination means (transistors 1001).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to impedance matching and load determination circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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